CS653A: Introduction to VLSI Design
Homework #1

Please use Cadence Virtuoso to draw transistor-level schematics of the following circuits, and then calculate the number of transistors used:

(1) An inverter (cell name: **inv**)
(2) A two-input NAND gate (cell name: **nand2**)
(3) A two-input NOR gate (cell name: **nor2**)
(4) A two-input AND gate (cell name: **and2**)
(5) A two-input OR gate (cell name: **or2**)
(6) A three-input NAND gate (cell name: **nand3**)
(7) A three-input NOR gate (cell name: **nor3**)
(8) An XOR gate (cell name: **xor**)
(9) A half-adder (cell name: **half_adder**)
(10) A full-adder (cell name: **full_adder**)
(11) An AOI22 gate (cell name: **aoi22**)
(12) A tristate inverter (cell name: **tri_inv**)
(13) A tristate buffer (cell name: **tri_buff**)
(14) A 2-input (2:1) multiplexer (cell name: **mux2**)
(15) A 4-input (4:1) multiplexer (cell name: **mux4**)
(16) A D latch (cell name: **d_latch**)
(17) A D flip-flop (cell name: **d_ff**)

Deadline: Tuesday, October 27th, 2009