CS653A: Introduction to VLSI Design
Homework #3

Deadline: Thursday, December 24th, 2009

Please complete the physical layouts of the following circuits:

(1) An inverter (cell name: **inv**)
(2) A two-input NAND gate (cell name: **nand2**)
(3) A two-input NOR gate (cell name: **nor2**)
(4) An XOR gate (cell name: **xor**)

Note that your layout designs must pass DRC, LVS, and post-layout simulations.